

REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Status of Claims:

Claims 1, 4, 9, 11, 15, 16, 18 and 21 are currently being cancelled.

Claims 5, 12 and 17 are currently being amended.

Claims 22-24 are being added.

This amendment and reply adds, cancels and amends claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claims remain under examination in the application, is presented, with an appropriate defined status identifier.

After adding, canceling and amending the claims as set forth above, claims 5, 12, 17 and 22-24 are now pending in this application.

Claim Rejections – 35 U.S.C. § 101:

In the Office Action, claim 12 is rejected under 35 U.S.C. § 101 as being to non-statutory subject matter, for the reasons set forth on page 9 of the Office Action. In reply, please note that claim 12 recites a step of: if the RT level description is determined to be acceptable, manufacturing the logic circuits based on the RT level description. Clearly, the manufacturing of logic circuits based on determining if an RT level description is acceptable recites useful, concrete and tangible results.

Accordingly, presently pending claim 12 is believed to fully comply with 35 U.S.C. § 101.

Claim Rejections – 35 U.S.C. § 112, 2nd Paragraph:

In the Office Action, claim 21 was rejected under 35 U.S.C. § 112, 2nd Paragraph, as being indefinite, for the reasons set forth on page 6 of the Office Action. While Applicant disagrees with the indefiniteness rejection of claim 21, that claim has been canceled to

expedite prosecution of this application, and to lessen the number of potential issues for appeal.

Claim Rejections – Prior Art:

In the Office Action, claims 1, 4-5, 9, 11-12, 15-18 and 21 were rejected under 35 U.S.C. § 102(a) as being anticipated by “Applied Boolean Equivalence Verification and RTL Static Sign-Off”, by Harry Foster; claims 1, 4-5, 9, 11-12, 15-18 and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by “As good as gold”, by Blackett; and claims 1, 4-5, 9, 11-12, 15-18 and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by “On the Formal Verification of ATM Switches”, by Jianping Lu. These rejections are traversed with respect to the presently pending claims under rejection, for at least the reasons given below.

Presently pending independent claim 5 has been amended to recite features described in numbered paragraphs 0076 and 0082 of the published U.S. patent application, whereby such features are not taught or suggested by the cited art of record.

Also, no comparing of first and second logic cones is performed in the system of Foster, so as to determine if an RT level description that has been designed in a behavioral synthesis phase is determined to be acceptable **to be used in a manufacturing phase for the logic circuits** when the first logic cones are logically equivalent to the second logic cones.

On page 7 of Foster, which is cited against certain features of claim 1, it merely describes BDD-based techniques for providing equivalence between different functions, whereby there is no teaching or suggestion of determining if first and second logic cones are logically equivalent in order to determine if an RT level description is acceptable to be used in a manufacturing phase for logic circuits. Similarly, page 9 of Foster, which is also cited against certain features of claim 1, merely describes Equivalence checking with don't cares, whereby it does not teach or suggest determining if first and second logic cones are logically equivalent in order to determine if an RT level description is acceptable to be used in a manufacturing phase for logic circuits.

Turning now to Blackett, the Office Action cites page 69, paragraph 1 and “A Practical Platform”, paragraphs 3 and 4 of that reference, for allegedly teaching certain

features of claim 1. Applicant respectfully disagrees. Namely, page 69 of Blackett merely describes a form of logic representation that overcomes the limitations of BDDs, whereby that form of logic representation includes logic cones. This high-level description of the use of logic cones falls well short of teaching or suggesting a means for determining if first and second logic cones are logically equivalent in order to determine if an RT level description is acceptable to be used in a manufacturing phase for logic circuits.

Turning now to Lu, the Office Action cites page 8, paragraph 3 of that reference, for allegedly teaching certain features of claim 1. Applicant respectfully disagrees. Namely, page 8 of Lu merely describes algorithms in which the traversal of output logic cones is done such that the combinational inputs farthest from the outputs appear earlier in the ordering. This high-level description of the use of logic cones falls well short of teaching or suggesting a means for determining if first and second logic cones are logically equivalent in order to determine if an RT level description is acceptable to be used in a manufacturing phase for logic circuits.

Since none of the cited references teaches the comparison of first and second logic cones to determine if they are logically equivalent, in order to determine if an RT level description is acceptable **to be used in a manufacturing phase for logic circuits.** Rather, the portions of the cited art of record provided on pages 3-7 of Foster, Blackett and Lu describes things that are done in a design verification phase.

Still further, if the techniques described in Foster, Blackett, and Lu are applied as they are, the following situations can be expected.

First, regarding the extraction of a logic cone from an object code, a user must directly specify which variable in which code portion of the object code is subjected to symbolic simulation. Second, the user must directly specify which one of the logic cones extracted from the object code and which one of the logic cones extracted from the RTL description are to be compared, by using the names of variables in the object code or the like.

However, in general, such specification is difficult to perform because object code is rather close to machine instructions, which is very difficult for a user to manipulate and analyze.

Foster, Blackett, and Lu do not disclose, teach or suggest a method or apparatus for making correspondences between these elements.

For example, the following statement can be found in Foster, page 7, line 5:

“Identifying all primary input and output pairs between the two FSMs.”

However, it is not disclosed in Foster how this identification is performed. Foster premises that the correspondences have been already given by some method, which Foster neglects to describe at all.

Moreover, the following statement can be found in Foster, page 8, the first paragraph of “Reducing complexity”:

“By exploiting the structural similarity between two designs, we can partition the combinational equivalence-checking problem into a set of smaller, simpler problems.”

However, Foster does not disclose or suggest any correspondence relation from behavioral synthesis or a method using compile information, in contrast to the present invention.

Furthermore, the following statement can be found in Foster, page 9-10, the first paragraph of “Sequential equivalence checking”:

The complexity of providing sequential equivalence is proportional to the design's state space. However, maintaining a consistent state space and state-encoding mapping between the specification and the implementation can reduce the complexity to a combinational equivalence-checking problem. Yet, in many cases, a one-to-one correspondence of the state space cannot be maintained. Examples include comparing a behavioral-level model to an RTL model or applying sequential transformations (such as retiring optimization) to a gate-level model. Hence, under these circumstances, sequential equivalence-checking techniques must be applied.”

Foster also does not disclose or suggest any correspondence relation from behavioral synthesis or a method using compile information, in contrast to the present invention.

The paragraph last mentioned above is followed by

“The process of proving sequential equivalence between two FSMs involves two steps. First, consistent presynchronization or transient behavior between the two machines must be established; ...”

which leads to

“These questions hint at the details of the various notions of machine equivalence, which are beyond the scope of this article. However, Huang and Cheng provide an excellent resource for the various equivalence definitions, as well as equivalence-checking techniques in general (such as incremental techniques, register correspondence, debugging, and error localization).

Further, the following statement can be found in Foster, page 12, the first paragraph of “Early and often”, in which it is described again that making correspondences is an important issue.

“First, designers can resolve name-mapping issues before sign-off. Earlier, I introduced the idea of exploiting structural similarity to reduce equivalence-checking complexity. Although many commercial equivalence checkers will use name-mapping techniques to identify structural similarity between designs, these algorithms are not perfect. User intervention is often required to resolve mapping issues. Waiting until the sign-off stage of design to resolve these issues is inviting trouble.”

Similarly, Blackett also describes that making correspondences is necessary, in the paragraph beginning with “Nor have any of these tools ...,” on page 68, but it does not disclose or suggest a method and apparatus in accordance with the presently claimed invention.

Accordingly, **the present invention resolves the above-described problems by using, in combination, the compile information indicating the correspondences between the behavioral level description and the object code, and the correspondence information indicating the correspondences between the behavioral level description and the RTL description.** These distinguishing features have been made more clear in presently pending independent claims 5, 12 and 17, whereby such features are not disclosed or suggested by the cited art of record.

Also, please note that, in the present invention, a user does not need to directly specify which one of the logic cones extracted by the first logic cone extraction section and which one of the logic cones extracted by the second logic cone extraction section are to be compared.

New Claims:

New independent claims 22-24 have been added to recite features with respect to compiler section (or corresponding method features) and a logic cone comparison section (or corresponding method features), whereby such features are not disclosed or suggested by the cited art of record.

Conclusion:

Since all of the issues raised in the Office Action have been addressed in this Amendment and Reply, Applicant believes that the present application is now in condition for allowance, and an early indication of allowance is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing or a credit card payment form being unsigned, providing incorrect information resulting in a rejected credit card transaction, or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

Date November 3, 2008

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